REMARKS

Claims 1-30 have been cancelled without prejudice. New claims 31-35 have been added.

Applicants appreciate the Examiner's acknowledgment of the claim for priority under 35 USC 119 and receipt of the foreign priority document.

The Examiner objected to Figs. 23-28, requiring them to be designated by a "Prior Art" legend. In reply, the Applicants request reconsideration, noting that Figs. 23-28 are included in the application to assist in the explanation of relevant prior art problems solved by the present invention. However, Figs. 23-28 show analysis by the present inventors which led to the improvements achieved by the present invention. Therefore, Figs. 23-28 are not properly considered prior art, and should not be designated as such.

A new title has been provided as required by the Examiner.

Claims 1-18 and 21-30 have been cancelled without prejudice or disclaimer. Therefore, the outstanding rejections under 35 USC 112 and 35 USC 102(b) have been rendered moot, with no admission as to the priority.

New claims 31-35, however, have been drafted with an eye to avoiding the problems noted by the Examiner noted on page

3, item 6, of the present Office Action. Further, claims 31-35 patently define over the applied patent to Fjelstad US 5,989,939, for the reasons which follow.

The sole independent claim 31 is directed to a method of manufacturing a semiconductor device, including steps of providing a film substrate, providing a plurality of semiconductor chips, arranging the semiconductor chips on device forming areas of the film substrate, electrically connecting electrodes of the semiconductor chips with electrode members on the device forming areas, forming a resin encapsulator to seal the device forming areas, electrode numbers, and semiconductor chips, and cutting the encapsulator and film substrate between adjacent device forming areas by dicing. The electrode members are spaced from the cutting surface resulting from the cutting step.

Claim 31 patentably defines over Fjelstad, which teaches a process of manufacturing compliant wirebond packages. The Examiner has noted that Fjelstad's Fig. 24, which is a top view of an embodiment in which a plurality of semiconductor chip assemblies are manufactured simultaneously. In the method depicted in Fig. 24, a semiconductor chip 44 is placed within each aperture 41 of a master frame 40. After forming a plurality of wire loops destined to become contacts, a

compliant material is disposed over the top surface of the master frame and the semiconductor chips. After curing the compliant material, the primary surface of the compliant layer is etched to expose the top portion of each wire loop. The master frame is then cut apart into a plurality of semiconductor chip assemblies, including one or more of the chips and adjacent parts of the frame.

Thus, one sees that Fjelstad does not disclose the combination of steps set forth in claim 31, including the steps of providing a film substrate having a plurality of device forming areas and electrode members on a main surface thereof, arranging a plurality of semiconductor chips on the device forming areas and electrically connecting the electrodes of the semiconductor chips with the electrode members on the device forming areas, forming a resin encapsulator collectively sealing the plurality of device forming areas, electrode members, and semiconductor chips, and cutting the resin encapsulator and film substrate between adjacent device forming areas by dicing, wherein the electrode members on the device forming areas of the film substrate main surface are spaced from the cutting edge resulting from the cutting step. Fjelstad discloses two separate semiconductor

chip assemblies, but no attention is paid to the positioning of the bond pads 42 with respect to the cutting surface.

Dependant claim 32 requires that the resin encapsulator containing the electrode members be separated from the film substrate, thereby revealing the electrode members on one side of the resin encapsulator before the cutting step is performed. Fjelstad neither discloses nor suggests that the bond pads 42 are exposed by the cutting step, nor that the encapsulated chip assembly is separated from the film substrate.

Dependent claim 33 requires that the cutting step include sticking dicing tape on another side of the resin encapsulator opposing the side of the resin encapsulator on which the electrode members are revealed. This feature is also neither disclosed nor suggested by Fjelstad.

Dependant claim 34 requires a step of plating the revealed electrode members after separating the resin encapsulator in claim 32. Again, Fjelstad does not suggest this step.

Finally, dependent claim 35 requires that the plating step be performed before the cutting step is performed. In Fjelstad, the cutting step is described without relation to

any step exposing or plating the bond pads 42. Accordingly, claim 35 is not shown in Fjelstad.

In view of the foregoing amendments and remarks, the Applicants request reconsideration of the rejection and allowance of the claims.

Respectfully submitted,

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